WHAT IS CLAIMED IS:

1. In a video processing circuit having an input stream of pixels corresponding to an array of video pixels, having a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array, having a video processing stage that inputs pixels using a fixed number of pixels, a method for delivering the input stream of pixels to the video processing stage, the method comprising:

establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels; and

concurrently

storing pixels from the input stream into a first set of line buffers, the pixels stored in the first set of line buffers including pixels for the established window size,

prefetching the stored pixels from the first set of line buffers into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size, and

for the video processing stage, fetching the fixed number of pixels from the second set of line buffers.

2. The method of claim 1, wherein each array of video pixels represents a video frame.

3. The method of claim 2, wherein the window size has X rows and Y columns, and the sampling-window size has X rows, where X is a fixed integer.

4. The method of claim 3, wherein establishing window size includes selecting Y from a set of possible integers.

5. The method of claim 4, wherein the fixed number of pixels equals 25, X equals 5 and the set of possible integers for Y is 1 through 4.

6. The method of claim 1, wherein the first set of line buffers is used to decouple the input stream of pixels from the second set of line of buffers.

7. The method of claim 1, wherein the second set of line buffers includes pixels that are addressed according to distance parameters defined relative to a current pixel.

8. The method of claim 7, wherein the distance parameters are defined according to the window size.

9. The method of claim 1, wherein the second set of line buffers includes pixels that are addressed according to distance parameters defined relative to a current pixel, wherein the distance parameters are defined according to a window size of X rows and Y columns, where X is a fixed integer and Y is selected to establish the sampling-window size.

10. The method of claim 1, wherein said respective line buffers have a length defined to optimize throughput and wherein said prefetching and said fetching includes passing pixel data through the respective line buffers to reduce cycle time.

11. The method of claim 1, wherein the window size has X rows and Y columns, where X is a fixed integer and Y is selected to establish the sampling-window size, and wherein the second set of line buffers includes X line buffers for respectively storing X rows of the pixels.

12. The method of claim 11, wherein the X line buffers of the second set of line buffers includes a center line buffer storing one row the pixels corresponding to a current line of the window, and at least one line buffer for storing another row of the pixels.

13. The method of claim 11, wherein the fixed number of pixels equals 25, X equals 5 and the set of possible integers for Y is 1 through 4.

14. In a video processing circuit having an input stream of pixels corresponding to an array of video pixels, having a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array, having a video processing stage that inputs pixels using a fixed number of pixels, a method for delivering the input stream of pixels to the video processing stage, the method comprising:

establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels; and

concurrently

decoupling the pixels from the input stream by using a first set of line buffers to store the pixels from the input stream, the pixels stored in the first set of line buffers including pixels for the established window size,

prefetching the stored pixels from the first set of line buffers into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size, and

for the video processing stage, fetching the fixed number of pixels from the second set of line buffers by addressing according to distance parameters defined relative to a current one of the pixels being stored in the second set of line buffers, wherein the distance parameters are defined according to a window size of X rows and Y columns, where X is a fixed integer and Y is selected to establish the sampling-window size.

15. A video processing circuit having an input stream of pixels corresponding to an array of video pixels, having a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array, having a video processing stage that inputs pixels using a fixed number of pixels, a circuit arrangement for delivering the input stream of pixels to the video processing stage, the circuit arrangement comprising:

means for establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels;

a first set of line buffers;

a second set of line buffers; and

means for concurrently

storing pixels from the input stream into the first set of line buffers, the pixels stored in the first set of line buffers including pixels for the established window size,

prefetching the stored pixels from the first set of line buffers into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size, and

for the video processing stage, fetching the fixed number of pixels from the second set of line buffers.

16. A video processing circuit having an input stream of pixels corresponding to an array of video pixels, having a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array, having a video processing stage that inputs pixels using a fixed number of pixels, a circuit arrangement for delivering the input stream of pixels to the video processing stage, the circuit arrangement comprising:

a programmable circuit for establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels;

a first set of line buffers;

a second set of line buffers; and

a data processing circuit configured and arranged to process video pixels by concurrently

storing pixels from the input stream into the first set of line buffers, the pixels stored in the first set of line buffers including pixels for the established window size,

prefetching the stored pixels from the first set of line buffers into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size, and

for the video processing stage, fetching the fixed number of pixels from the second set of line buffers.

17. The circuit arrangement of claim 16, wherein each array of video pixels represents a video frame.

18. The circuit arrangement of claim 17, wherein the window size has X rows and Y columns, and the sampling-window size has X rows, where X is a fixed integer.

19. The circuit arrangement of claim 18, wherein the programmable circuit is adapted to select Y from a set of possible integers.

20. The circuit arrangement of claim 19, wherein the fixed number of pixels equals 25, X equals 5 and the set of possible integers for Y is 1 through 4.

21. The circuit arrangement of claim 16, wherein the first set of line buffers is used to decouple the input stream of pixels from the second set of line of buffers.

22. The circuit arrangement of claim 16, wherein the second set of line buffers includes pixels that are addressed according to distance parameters defined relative to a current pixel.

23. The circuit arrangement of claim 22, wherein the distance parameters are defined according to the window size.

24. The circuit arrangement of claim 16, wherein the second set of line buffers includes pixels that are addressed according to distance parameters defined relative to a current pixel,

wherein the distance parameters are defined according to a window size of X rows and Y columns, where X is a fixed integer and Y is selected to establish the sampling-window size.

25. The circuit arrangement of claim 16, wherein said respective line buffers have a length defined to optimize throughput and wherein the data processing circuit is further configured and arranged to said pass pixel data through the respective line buffers to reduce cycle time.

26. The circuit arrangement of claim 16, wherein the window size has X rows and Y columns, where X is a fixed integer and Y is selected to establish the sampling-window size, and wherein the second set of line buffers includes X line buffers for respectively storing X rows of the pixels.

27. The circuit arrangement of claim 26, wherein the X line buffers of the second set of line buffers includes a center line buffer storing one row the pixels corresponding to a current line of the window, and at least one line buffer for storing another row of the pixels.

28. The circuit arrangement of claim 26, wherein the fixed number of pixels equals 25, X equals 5 and the set of possible integers for Y is 1 through 4.